Electronic Version
Stylesheet Version v1.1.1

Description

[METHOD FOR DETECTING DEFECT OF SEMICONDUCTOR DEVICE]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] This invention generally relates to a method of detecting semiconductor device, and more particularly to a method of detecting defect of a semiconductor device.

[0003] Description of the Related Art

[0004] An integrated circuit integrates devices and circuit into a 2cm x 2cm or smaller area. Because it generally includes more than ten thousand solid-state devices, an integrated circuit is so called a microelectronic device. If a microelectronic device has a defect, the microelectronic device may not operate properly. Further, when the size of the device becomes smaller, it is very difficult to improve the yield rate. One of the key issues regarding the yield rate is the defect in the microelectronic device. Therefore, how to

detect and reduce the defects is a very important issue in improving the yield rate.

[0005] The conventional method of detecting defects is to decap each layer of the device by etching and to analyze the defects in each layer. That is, the conventional method removes each layer from top to bottom and finds out the defects in each layer until the bottom layer of the device.

[0006] However, as the integration level of the device increases, the conventional method may not be applicable, especially for detecting the defects generated during the front-end process, because it takes a long time to decap each layer to find out if there is any defect in a particular layer. Further, the defect may be removed during the etching process so that the defect cannot be detected any more.

SUMMARY OF INVENTION

[0007] An object of the present invention is to provide a method of detecting defect of semiconductor device in order to precisely and quickly detect the defects in the device.

[0008] The present invention provides a method of detecting defect of semiconductor device. The semiconductor device at least includes a substrate, a gate, a source region, a drain region, a plug, an insulating layer and a conducting line. The plug electrically connects the source region or

the drain region and is located above a portion of the gate. At least a defect exists between the plug and the gate. The method comprises: polishing the semiconductor device until the plug is not above the portion of the gate; cleaning the semiconductor device; removing the insulating layer between the gate and the plug; and detecting the defect between the plug and the gate.

[0009] In a preferred embodiment of the present invention, the polishing step further comprises polishing the semiconductor device to partially expose the gate. The cleaning step comprises using deionized water to clean the semiconductor device and drying the semiconductor device. The removing step comprises performing a wet etching process and performing a dry etching process.

[0010] The present invention polishes the semiconductor device until the plug above the gate is substantially removed and then the insulating layer between the gate and the plug is removed. Hence, the method of the present is capable of eliminating the defects occurring from removal steps using the wet etching processes and therefore the defect can be precisely and effectively detected.

[0011] The present invention provides a method of detecting defect of semiconductor device. The semiconductor device

at least includes two adjacent conducting layers and an insulating layer. The insulating layer is disposed between the two adjacent conducting layers, wherein a defect exists between the two adjacent conducting layers. The method comprises: polishing the semiconductor device to partially expose the two adjacent conducting layers; removing the insulating layer between the two adjacent conducting layers; and detecting the defect between the two adjacent conducting layers.

[0012] In a preferred embodiment of the present invention, after the polishing step and before the removing step, the method further comprises cleaning the semiconductor device. The cleaning step comprises using deionized water to clean the semiconductor device and drying the semiconductor device. The removing step comprises a wet etching process or a dry etching process.

[0013] In a preferred embodiment of the present invention, the semiconductor device is polished until the two adjacent conducting layers are partially exposed and then the insulating layer between the two adjacent conducting layers is removed. Hence, the method of the present invention is capable of preventing the defect occurring due to removal steps using wet etching process, and therefore the defect

can be precisely and effectively detected.

[0014] The above is a brief description of some deficiencies in the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims.

Brief Description of Drawings

[0015] FIGs.1A-1C are cross-sectional views illustrating the process for detecting the defects in a semiconductor device in accordance with a preferred embodiment of the present invention.

[0016] FIGs.2A-2B are scanning electron microscope photographs of a semiconductor device in accordance with Experiment 1of the present invention.

[0017] FIGs.3A-3B are scanning electron microscope photographs of a semiconductor device in accordance with Experiment 2 of the present invention.

[0018] FIGs.4A-4B are scanning electron microscope photographs of a semiconductor device in accordance with Comparison 1 of the present invention.

[0019] FIGs.5A-5B are scanning electron microscope photographs of a semiconductor device in accordance with

another experiment of the present invention.

DETAILED DESCRIPTION

[0020] FIGs.1A-1C are cross-sectional views illustrating the process for detecting the defects in a semiconductor device in accordance with a preferred embodiment of the present invention.

[0021] Referring to FIG. 1A, a semiconductor device 100 includes a substrate 102, a gate 104, a passivation layer 106, a plug 108, an insulating layer 110, a bit line 112, and a stack layer 114.

[0022] The plug 108 electrically connects with the source region or the drain region 116 and is located above a portion of the gate 104. A defect 118 exists between the plug 108 and the gate 104. The defect 118 is, for example, a conductive particle which may cause a short between the plug 108 and the gate 104, such as, for example, a nanomemter scale defect. The passivation layer 106 is comprised of, for example, a TEOS silicon oxide layer and a silicon nitride layer. The insulating layer 110 is comprised of, for example, a TEOS silicon oxide layer. The stack layer 114 includes a capacitor, the insulating layer, the plug, and the conducting line layer above the bit line 112. For simplicity, in this embodiment, the stack layer

114 is used to represent the subsequent layers formed above the bit line.

[0023] Referring to FIG. 1B, a polishing step is performed to polish the semiconductor device 100 until the plug 106 above the gate 104 is substantially removed. In this polishing step, the polishing machine is, for example, a dimple grinder, Model 656N, JOEL Ltd. Alternatively, the polishing step is performed until the gate 104 is partially exposed. Then a cleaning step is performed to clean the semiconductor device 100. During the cleaning step, deionized water is used to clean the semiconductor device 100 and then the semiconductor device 100 is dried. The cleaning step usually takes about 5-10 seconds.

[0024] Referring to FIG. 1C, a removing step is performed to remove the insulating layer 110 and the passivation layer 106 between the gate 104 and the plug 108. Preferably, the removing step includes a wet etching process which is performed by using HF as an etchant to remove the TEOS silicon oxide. Then a dry etching process such as reactive ion etching process is performed to remove the silicon nitride layer and the TEOS silicon oxide. In this step, because the defect 118 usually is a conductive particle, it will not be removed. Further, after removing the passiva-

tion layer 106 and the insulating layer 110 located between the gate 104 and the plug 108, a cleaning step is performed. Thereafter, the defect 118 between the plug 108 and the gate 104 can be detected. To detect the defect, a scanning electron microscope could be used.

[0025] In the above embodiment, a defect between the plug and the gate is used as an example to illustrate the method of the present invention. However, the method of the present invention also can be applied to detect the defect between the conducting layers (conducting lines). For example, to detect the defect between the conducting layers, a polishing step is performed to polish the semiconductor until two adjacent conducting layers are exposed. Then the insulating layer between two adjacent conducting layers is removed by using a wet or a dry etching process. A scanning electron microscope then is used to detect the defect between two adjacent conducting layers.

[0026] To illustrate the advantages of the present invention, Experiment 1, Experiment 2, and Comparison 1 are used to further describe the method of the present invention. A DRAM is used in Experiment 1, Experiment 2, and Comparison 1.

[0027] <Experiment 1>A semiconductor chip (a DRAM chip) hav-

ing a critical dimension of 0.15 μm is provided. The chip is polished until the plug above the gate is substantially removed. In this polishing step, the polishing time is about 12 minutes. After the chip is cleaned, the insulating layer between the plug and the gate is removed. In this step, a wet etching step is performed for 1 minute by using HF as an etchant. After the insulating layer is removed, the chip is cleaned again. Then a scanning electron microscope is used to detect the defect between the plug and the gate. The results are shown in FIGs. 2A-2B, which show the cell area of the DRAM.

[0028] <Experiment 2>A semiconductor chip (a DRAM chip) having a critical dimension of 0.13 μm is provided. The same steps are performed in this experiment on the chip as in Experiment 1. Then a scanning electron microscope is used to detect the defect between the plug and the gate. The results are shown in FIGs. 3A-3B, which show the cell area of the DRAM.

[0029] <Comparison 1>A semiconductor chip (a DRAM chip) having a critical dimension of 0.15 μm is provided. First, a wet etching process using HF as an etchant is performed for 3 minutes to remove the conducting layer. Then a cleaning step is performed. Next, a wet etching process

using H_2SO_4 as an etchant is performed for 10 minutes to remove the top cell plate layer.

[0030] To remove the storage node layer, a reactive ion etching process is performed for 2 minutes to remove the silicon nitride/silicon oxide/ silicon nitride dielectric layer. A wet etching process using HF as an etchant is performed for 5 mins to further remove the silicon nitride/silicon oxide/ silicon nitride dielectric layer and to remove the insulating layer. The bottom cell plate layer is removed by using KOH as an etchant for 15 seconds. A wet etching process using HF as an etchant is performed for 5 minutes to further remove the bottom cell plate layer.

[0031] To remove the bit line and the plug, a wet etching process using H_2SO_4 as an etchant is performed for 10 minutes to remove the metal layer. The polysilicon layer is removed by using KOH as an etchant for 20 seconds. A wet etching process using HF as an etchant is performed for 5 minutes to further remove the remaining bit line and the plug. After removing the bit line and the plug, a scanning electron microscope is used to detect the defect between the plug and the gate. The results are shown in FIGs. 4A-4B, which show the cell area of the DRAM. It should be noted that after each removing step, a cleaning step would be per-

formed.

[0032] By analyzing the results in Experiments 1 and 2 shown in FIGs. 2B and 3B, the defects can be clearly observed between the gate and the plug. Further, the present invention also can be applied to the device having a smaller critical dimension. However, the result indicated in Comparison 1 (FIG. 4B) cannot show the defect between the plug and the gate. This is because the defect is usually a conductive particle. During the removal of the plug using wet etching process, the defect is also removed. Hence, the defect cannot be defected in FIG. 4B.

[0033] Further, Experiments 1 and 2 take about 15 minutes to detect the defect. However, Comparison 1 takes at least 30 minutes. Hence, the method of the present invention can save more time than the conventional method.

[0034] Further, FIGs.5A-5B are the scanning electron microscope photographs of a semiconductor device in accordance with another experiment of the present invention. As shown in FIGs. 5A-5B, the defect between the plug and the gate is clearly shown.

[0035] In Experiment 1, Experiment 2, and Comparison 1, the DRAM is used as examples. However, the present invention can also be applied to detect the defects of the pe-

ripheral circuit of the DRAM or other semiconductor devices.

[0036] In the embodiment of the present invention, the semiconductor device subjected to a polishing step until the plug above the gate is substantially removed and then the insulating layer between the gate and the plug are removed. Hence, the method of the present invention is capable of preventing the defect occurring due to the wet etching process and therefore the defect can be precisely and effectively detected.

[0037] The above description provides a full and complete description of the preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is defined by the following claims.